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Attorneys for Plaintiffs and Counterdefendants
ALPHA & OMEGA SEMICONDUCTOR, LTD.
ALPHA & OMEGA SEMICONDUCTOR, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation; and ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C-07-2664 JSW)

DECLARATION OF YALEI SUN IN SUPPORT OF ALPHA & OMEGA SEMICONDUCTOR, LTD AND ALPHA & OMEGA SEMICONDUCTOR, INC'S OPPOSITION CLAIM CONSTRUCTION BRIEF PURSUANT TO CIVIL L. R. 16-11(D)(1)

Date: June 4, 2008
Time: 2:00 PM
Place: Courtroom 2, 17th Floor
Judge: Honorable Jeffrey S. White

I, Yalei Sun, hereby declare as follows:

1. I am an associate at the law firm of Morgan, Lewis & Bockius LLP, 2 Palo Alto Square Avenue, 3000 El Camino Real, Suite 700, Palo Alto, California 94306, and a member in good standing of the Bar of the State of California. Morgan, Lewis & Bockius LLP has been retained as trial counsel for the Plaintiffs and Counterdefendants Alpha & Omega Semiconductor, LTD and Alpha & Omega Semiconductor, Inc., in the present action. I submit this declaration in support of Alpha & Omega Semiconductor, LTD and Alpha & Omega Semiconductor, Inc.'s Opposition Claim Construction Brief Pursuant to Civil L. R. 16-11(d)(1).

2. Attached hereto as Exhibit 1 is a true and correct copy of United States Patent No. 6,429,481.

3. Attached hereto as Exhibit 2 is a true and correct copy of United States Patent No. 6,710,406.

4. Attached hereto as Exhibit 3 is a true and correct copy of United States Patent No. 6,521,497.

5. Attached hereto as Exhibit 4 is a true and correct copy of United States Patent No. 6,828,195.

6. Attached hereto as Exhibit 5 is a true and correct copy of United States Patent No. 7,148,111.

7. Attached hereto as Exhibit 6 is a true and correct copy of United States Patent No. 6,818,947.

8. Attached hereto as Exhibit 7 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,429,481, Application as Filed.

9. Attached hereto as Exhibit 8 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,429,481, Amendment received by the Patent Office November 8, 1999.

10. Attached hereto as Exhibit 9 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,429,481, Amendment received by the Patent Office September 5, 2000.

11. Attached hereto as Exhibit 10 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,429,481, Office Action dated December 5, 2000.

12. Attached hereto as Exhibit 11 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,429,481, Amendment received by the Patent Office June 7, 2001.[1]

13. Attached hereto as Exhibit 12 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,429,481, Amendment received by the Patent Office December 31, 2001.

14. Attached hereto as Exhibit 13 is a true and correct copy of the Appeal Brief for Application No. 10/630,249 dated November 3, 2005.

15. Attached hereto as Exhibit 14 is a true and correct copy of pages 63 – 108 of S.M. Sze, *Physics of Semiconductor Devices* (1981) (describing abrupt and linearly graded P-N junctions and the differences between the two).

16. Attached hereto as Exhibit 15 is a true and correct copy of page 1 of THE IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS (6th ed. 1997) (defining "abrupt junction").

17. Attached hereto as Exhibit 16 is a true and correct copy of page 1 of the MCGRAW-HILL ELECTRONICS DICTIONARY (5th ed. 1994) (defining "abrupt junction").

18. Attached hereto as Exhibit 17 is a true and correct copy of pages 63 – 70, and 298 of Sorab K. Ghandhi, *Semiconductor Power Devices* (1977) (describing field termination structures and identifying a high-low junction as an ohmic contact where current flows easily in either direction).

19. Attached hereto as Exhibit 18 is a true and correct copy of pages 210, 446 – 455 of R.W. Warner and G.L. Grung, *TRANSISTORS : Fundamentals for the Integrated Circuit Engineer* (1990) (identifying a high-low junction as an ohmic contact where current flows easily on either direction).

20. Attached hereto as Exhibit 19 is a true and correct copy of pages 116 – 119 of B. Jayant Baliga, Modern Power Devices (1992) (describing the operation of field plates).

21. Attached hereto as Exhibit 20 is a true and correct copy of United States Patent No. 5,233,215 (cited by the '947 patent for its description of trenched field plates).

[1],Note that the original page 4 of this document was apparently missing from the file wrapper at the Patent Office. The current copy of page 4 was produced by Fairchild from its own photocopy of the same document in response to AOS's request.

22. Attached hereto as Exhibit 21 is a true and correct copy of page 2065 of the MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS (5th ed. 1994) (defining "trench").

23. Attached hereto as Exhibit 22 is a true and correct copy of page 1259 of Merriam Webster's Collegiate Dictionary (10th ed. 1997) (defining "trench").

24. Attached hereto as Exhibit 23 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,818,947, Amendment received at the Patent Office July 21, 2003.

25. Attached hereto as Exhibit 24 is a true and correct copy of the Prosecution History of U.S. Patent No. 6,818,947, Amendment received at the Patent Office December 29, 2003.

26. Attached hereto as Exhibit 25 is a true and correct copy of pages 0 – 3, 204 – 212 of AOS's Supplemental Preliminary Invalidity Contentions for U.S. Patent Nos. 6,429,481, 6,521,497, 6,710,406, 6,828,195, 7,148,111, and 6,818,947 Pursuant to Patent L.R. 3-3, served March 3, 2008.

27. Attached hereto as Exhibit 26 is a true and correct copy of the definition of "Finite element analysis" from Wikipedia, (http://en.wikipedia.org/wiki/Finite_element_analysis), downloaded January 7, 2008.

28. Attached hereto as Exhibit 27 is a true and correct copy of Exhibit 2 of Fairchild's Preliminary Infringement Contentions.

29. Attached hereto as Exhibit 28 is a true and correct copy of pages 0 – 3, 207 – 209 of AOS's Preliminary Invalidity Contentions For U.S. Patent Nos. 6,429,481, 6,521,497, 6,710,406, 6,828,195, 7,148,111, and 6,818,947 Pursuant to Patent L.R. 3-3, served November 29, 2007.

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I declare under of penalty of perjury that the foregoing is true and correct. Executed in Palo Alto, California.

Dated: March 27, 2008

by _____
Yalei Sun